IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/647,018 Group Art Unit: 2138

Filed: August 22, 2003 Examiner: Dipakkumar Gandhi

Applicant: Zahi Abuhamdeh, et al. Attorney Docket: TRA-078

Title: Microprocessor Based Self-Diagnostic Port

Commissioner for Patents
Alexandria, VA 22313

Sir:

APPLICANT'S REPLY BRIEF

The Examiner's Answer to the Applicant's Brief on Appeal was mailed on September 11, 2007 making this Reply Brief timely.

Status of the Claims

This application was filed with claims 1-20. There have been no amendments to or cancellations of the claims. All claims stand finally rejected. The final rejection of claims 1-20 was appealed on September 18, 2006. Therefore, claims 1-20 are the claims on appeal.

Grounds for Rejection to be Reviewed on Appeal

Prior to the filing of the Examiner's Answer, the sole issue on appeal is whether claims 1-20 are unpatentable under 35 U.S.C. §103(a) as obvious over Texas Instruments Document SCBS676D-December 1996-Revised August 2002 (hereinafter "Texas Instruments") in view of Patavalis.

The Examiner's Answer raises the issues of whether it would have been obvious to combine JTAG TAP, JTAG Master, and core logic on a single chip to implement the IEEE 1149.1 standard "without need for additional logic or buffering and achieve the predictable results of reducing signal processing time."

Argument

During prosecution and in the Applicant's Brief, the Applicant has emphasized that the claimed invention is directed to a single chip which includes both a JTAG TAP and a JTAG Master, as well as core logic. The Examiner has previously ignored that fact that the invention places these elements on a single chip whereas the prior art specifically teaches not to place these elements on a single chip. The Examiner has finally addressed this issue in his Answer to the Applicant's Brief.

The Examiner now states for the first time that it would have been obvious to combine these elements on a single chip to implement the IEEE 1149.1 standard "without need for additional logic or buffering and achieve the predictable results of reducing signal processing time." See pages 8, 11, 12, 13, 14, 15, 16, 17, 18, and 20 of the Examiner's Answer where this new argument is made repeatedly.

In response to this new argument, the Applicant would like to point out that the claimed invention is not obvious because the prior art actually teaches away from the claimed combination and that the invention achieves not predictable results but unexpected results.

The Examiner's new argument seems to rest on the assumption that placing multiple components on a single chip will always result in "reduced signal processing time". It is also based on the assumption that reduced signal processing time is a desirable

goal in implementing the IEEE 1149.1 standard. The Examiner has made no showing that reduced signal processing time would be a result nor has he made any showing that such a result would be desirable or even relevant.

Clearly, there are many factors which determine signal processing time, one of which is the clock rate of the processor. There is no reason to believe that merely putting more circuitry on a single chip will reduce signal processing time.

An examination of the literature regarding the IEEE 1149.1 standard reveals that there is no discussion or reference to signal processing time. Thus, one may justly assume that signal processing time is not an issue in the implementation of the IEEE 1149.1 standard. This is further supported by the fact that the IEEE 1149.1 standard is not directed to real time signal processing where latency is an issue. The IEEE 1149.1 standard is directed to a testing method in which latency is not an issue.

Reduced signal processing time was not the goal of the invention nor is it a stated result of the invention. The actual results of combining elements on a single chip are set out in some detail at pages 5 and 6 of the instant specification. By the Examiner's own tacit admission, these results are "unexpected".

The present invention allows diagnostic testing of a chip on a circuit board without removing the chip from the board or taking the board out of service. This is not an expected result as it is not related to "reduced signal processing time".

The present invention also enables chip manufacturers to provide a single testing solution for the chip which will work properly regardless of the board on which the chip is used. This is not an expected result as it is not related to "reduced signal processing time".

The invention further provides for selecting between standard JTAG testing and testing according to the invention. This is not an expected result as it is not related to "reduced signal processing time".

Using the invention, board developers and device maintenance personnel can perform the same diagnostic tests as the chip manufacturer to determine whether the chip is performing according to specification. This is not an expected result as it is not related to "reduced signal processing time".

The invention also allows more accurate tests of in-service boards which are part of a larger device, e.g. a telecommunications switch. This is not an expected result as it is not related to "reduced signal processing time".

With the invention, a chip manufacturer can supply developers with a set of diagnostic programs which can be used to test the chip regardless of how the board carrying the chip is designed. This is not an expected result as it is not related to "reduced signal processing time".

The present implementation of the invention allows the same JTAG master and microprocessor interface to be used on many different chips without modification. This is not an expected result as it is not related to "reduced signal processing time".

Not only does the claimed invention provide all of these unexpected results, it does so by ignoring the conventional wisdom. The prior art actually teaches away from placing these three elements (JTAG TAP, JTAG Master, and core logic) all on the same chip. All of the references to the JTAG standard (IEEE 1149.1) always show the JTAG TAP and the JTAG Master on separate chips. Thus, the prior art teaches away from the claimed invention.

In light of all of the above, it is submitted that the claims are in order for allowance, and the applicant respectfully requests that the Board direct the Examiner to allow the case.

Respectfully submitted,

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